SUPPORT FOR AMENDMENTS

The claims have been clarified; the amendment is supported by the figures. No new matter has been added. Upon entry of this amendment claims 1-19 and 23-26 are present and active in the application.

REQUEST FOR RECONSIDERATION

Applicant would like to thank Examiner Mitchell for the courteous and helpful discussion held with Applicant's representative on October 22, 2004. During this discussion, specific language to replace the word "on" throughout the claims, so as to achieve the meaning applicants intended, was discussed. Accordingly, the phrase "supported by" has now been used to replace "on" in all the claims.

A widely used isolation technique in semiconductor structures, silicon trench isolation (STI) traditionally includes forming a screen SiO_2 layer supported by a semiconductor substrate, followed by depositing an isolation Si_3N_4 layer over the screen SiO_2. A photoresist is then deposited and the structure is etched, opening a trench in the substrate. The photoresist is stripped, an oxide layer is deposited, and the structure is planarized via CMP. The isolation Si_3N_4 layer is then etched away.

A problem with STI is the low uniformity of the surface after CMP, which renders overetching the isolation Si_3N_4 layer necessary in order to remove all the nitride. This results in a non-uniform thickness of the underlying screen SiO_2 layer, which negatively affects the consistency of the threshold voltages of the transistors on the wafer.

The present invention addresses this problem by providing an STI method that includes covering the semiconductor substrate with a new type of isolation region. As shown in Figure 6, this region has a first sacrificial oxide layer **118** over the screen SiO_2 layer **110** and the isolation Si_3N_4 layer **106** over the sacrificial oxide layer. An optional second Si_3N_4 sacrificial layer **120** can also be part of the isolation region.

With this new type of structure, the first sacrificial layer protects the screen SiO_2 layer from the overetching of the isolation Si_3N_4 layer, thus leading to a product with a more uniform surface (page 4, line 20, to page 5, line 23).

The rejections of the claims over Lou et al. are respectfully traversed. The nitride layer of Lou et al. is not supported by the sacrificial layer.

Lou et al. provides a method where an isolation Si_3N_4 layer **14** is in contact with a screen SiO_2 layer **12** (Figure 1). An oxide layer **19** is present, which lines the trench, and lays over the SiO_2 layer **12** and the Si_3N_4 layer **14** (Figure 1). This layer is formed by thermal oxidation, and therefore forms only along exposed surfaces (col. 2, lines 42-48). At no point is the nitride layer **14** supported by this oxide layer **19**: the oxide layer

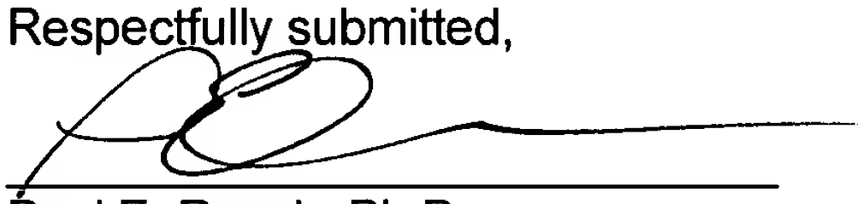
19 is adjacent and supported by the nitride layer **14**. After the etching and the depositing of the dielectric filler **20**, the structure of Lou et al. is subjected to a two-stage CMP step (col.2, lines 49-60) yielding the structure of Figure 2B which is then processed to the final product.

As claimed, the present invention includes a nitride layer supported by a sacrificial layer. In contrast, Lou et al. includes an oxide layer **19** which is formed after the nitride layer **14**, so that the nitride layer cannot be supported by the oxide layer **19**. Consequently, Lou et al. neither teaches nor suggests the method of the claimed invention. Withdrawal of these grounds of rejection is respectfully requested.

The rejection of claims 20 and 21 is moot, since these claims were cancelled in a previous response.

Applicant submits that the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



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